TSMC-02-1330

March 19, 2004

To: Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: Serial No. 10/767,276 01/29/04

Kern-Huat Ang et al.

METHOD FOR END POINT DETECTION OF POLYSILICON CHEMICAL MECHANICAL POLISHING IN AN ANTI-FUSE MEMORY DEVICE

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on March 25, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date Stephen B. Ackerman 3/25/04

U.S. Patent 5,670,410 to Pan, "Method of Forming Integrated CMP Stopper and Analog Capacitor," teaches a method to form an analog capacitor with a topmost electrode comprising polysilicon.

U.S. Patent 6,391,768 to Lee et al., "Process for CMP Removal of Excess Trench or Via Filler Metal which Inhibits Formation of Concave Regions on Oxide Surface of Integrated Circuit Structure," describes a method to chemical mechanical polish a metal layer overlying a dielectric layer.

U.S. Patent 6,261,851 to Li et al., "Optimization of CMP Process by Detecting of Oxide/Nitride Interface Using IR Sytem," describes a method and an apparatus to detect and to monitor ammonia gas given off as a bi-product in a CMP operation.

U.S. Patent 6,294,457 to Liu, "Optimized IMD Scheme for Using Organic Low-K Material as IMD Layer," describes a method to prevent particle contamination during an argon (Ar) sputter operation used for pre-cleaning metal.

U.S. Patent 6,008,104 to Schrems, "Method of Fabricating a Trench Capacitor with a Deposited Isolation Collar," discusses a trench capacitor achieved by providing a node dielectric that lines the collar and sidewalls of the bottom of the trench.

U.S. Patent 6,423,628 to Li et al., "Method of Forming Integrated Circuit Structure having Low Dielectric Constant Material and having Silicon Oxynitride Caps Over Closely Spaced Apart Metal Lines," discloses a capping layer of an insulator such as silicon oxynitride formed over horizontally closely spaced apart metal lines on an oxide layer of an integrated circuit structure formed on a siemconductor substrate.

U.S. Patent 6,531,410 to Bertin et al., "Intrinsic Dual Gate Oxide MOSFET Using a Damascene Gate Process," discusses dual gate oxide MOSFET using a damascene gate process.

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761

Sheet 1 of 1

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

MAR 2 9 2004 PATENT & TRADEMARK OFFICE

Docket Number (Optional)	Application Number
TSMC-02-1330	10/767,276
Applicant: Kern-Huat Ang et al.	
Filing Date: 01/29/04	Group Art Unit:

U. S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	5670410	9/23/97	Pan	437	60	9/25/96
	6391768	5/21/02	Lee et al.	438	633	10/30/00
	6261851	7/17/01	Li et al.	438	8	9/30/99
	6294457	9/25/01	Liu	438	623	2/1/01
	6423628	7/23/02	Li et al.	438	622	10/22/99
	6008104	12/28/99	Schrems	438	386	4/6/98
	6531410	3/11/03	Bertin et al.	438	766	2/27/01

FOREIGN PATENT DOCUMENTS

	Document Number	Date	Country	Class	Subclass	Translation YES	Translation NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

Examiner	Date Considered

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant